N-Channel Power MOSFET 500 V, 0.52 Ω

Features

- Low ON Resistance
- Low Gate Charge
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	NDF	NDP	Unit
Drain-to-Source Voltage	V_{DSS}	500		V
Continuous Drain Current, $R_{\theta JC}$ (Note 1)	I _D	12		А
Continuous Drain Current $T_A = 100^{\circ}C$, $R_{\theta JC}$ (Note 1)	I _D	7.4		Α
Pulsed Drain Current, t _P = 10 μs	I _{DM}	44		Α
Power Dissipation, $R_{\theta JC}$	P_{D}	39	178	W
Gate-to-Source Voltage	V_{GS}	±30		V
Single Pulse Avalanche Energy, I _D = 10 A	E _{AS}	420		mJ
ESD (HBM) (JESD22-A114)	V _{esd}	4000		V
RMS Isolation Voltage (t = 0.3 sec., R.H. \leq 30%, T _A = 25°C) (Figure 14)	V _{ISO}	4500		٧
Peak Diode Recovery	dv/dt	4.5 (Note 2)		V/ns
Continuous Source Current (Body Diode)	I _S	12		Α
Maximum Temperature for Soldering Leads	TL	260		°C
Operating Junction and Storage Temperature Range	T _J , T _{stg}	–55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

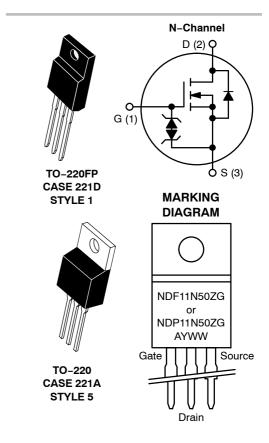
- 1. Limited by maximum junction temperature
- 2. $I_d \le 10.5 \text{ A}$, $di/dt \le 200 \text{ A}/\mu s$, $V_{DD} \le BV_{DSS}$, $T_J \le 150 ^{\circ} C$.



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V _{DSS}	R _{DS(ON)} (MAX) @ 4.5 A
500 V	0.52 Ω



A = Location Code

Y = Year WW = Work Week

G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

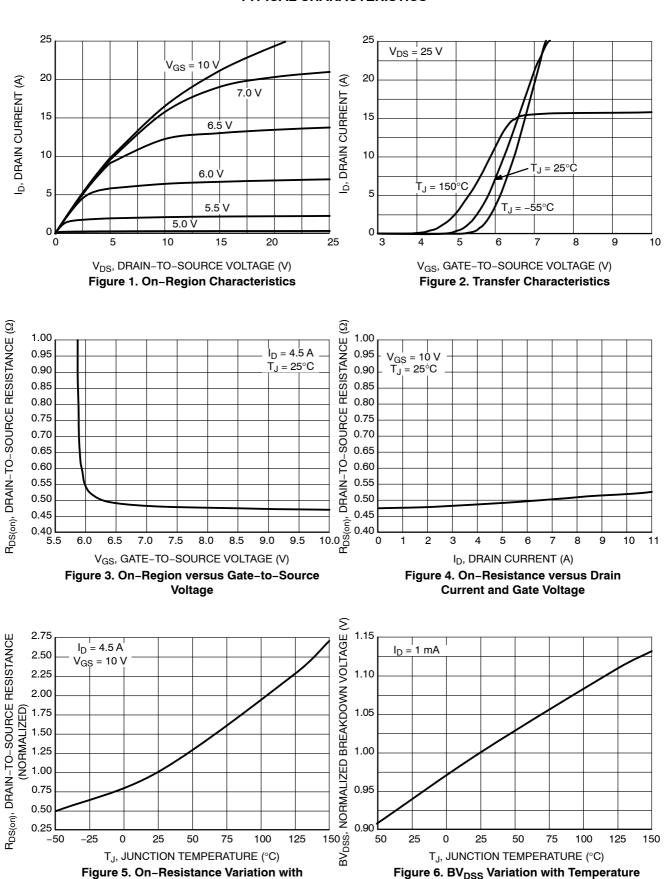
THERMAL RESISTANCE

Parameter	Symbol	NDF11N50Z	NDP11N50Z	Unit
Junction-to-Case (Drain)	$R_{ heta JC}$	3.2	0.7	°C/W
Junction-to-Ambient Steady State (Note 3)	$R_{\theta JA}$	50	50	

Characteristic	Test Conditions		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			•		•		
Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ m/s}$	4	BV _{DSS}	500			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D = 1 mA		$\Delta BV_{DSS}/ \ \Delta T_{J}$		0.6		V/°C
Drain-to-Source Leakage Current		25°C	I _{DSS}			1	μΑ
	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	125°C	1			50	
Gate-to-Source Forward Leakage	V _{GS} = ±20 V		I _{GSS}			±10	μА
ON CHARACTERISTICS (Note 4)							
Static Drain-to-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 4.5$	A	R _{DS(on)}		0.48	0.52	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 100 \mu A$		V _{GS(th)}	3.0		4.5	V
Forward Transconductance	V _{DS} = 15 V, I _D = 4.5 A		9FS		7.7		S
OYNAMIC CHARACTERISTICS					-		
Input Capacitance			C _{iss}		1375		pF
Output Capacitance	$V_{DS} = 25 \text{ V, } V_{GS} = 0 \text{ V,}$ $f = 1.0 \text{ MHz}$		C _{oss}		166]
Reverse Transfer Capacitance			C _{rss}		40		
Total Gate Charge			Q_g		46		nC
Gate-to-Source Charge	V _{DD} = 250 V, I _D = 10.5	Α,	Q_gs		8.7		
Gate-to-Drain ("Miller") Charge	$V_{GS} = 10 \text{ V}$		Q_{gd}		25		
Plateau Voltage			V_{GP}		6.2		V
Gate Resistance			R_g		1.4		Ω
RESISTIVE SWITCHING CHARACTER	STICS				-		
Turn-On Delay Time	V_{DD} = 250 V, I_{D} = 10.5 A, V_{GS} = 10 V, R_{G} = 5 Ω		t _{d(on)}		15		ns
Rise Time			t _r		32		
Turn-Off Delay Time			t _{d(off)}		40		
Fall Time			t _f		23		
OURCE-DRAIN DIODE CHARACTER	ISTICS (T _C = 25°C unless oth	erwise not	ed)	_			
Diode Forward Voltage	I _S = 10.5 A, V _{GS} = 0 V		V_{SD}			1.6	V
Reverse Recovery Time	$V_{GS} = 0 \text{ V}, V_{DD} = 30 \text{ V}$ $I_{S} = 10.5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		t _{rr}		310		ns
						4	

Insertion mounted
 Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS



Temperature

TYPICAL CHARACTERISTICS

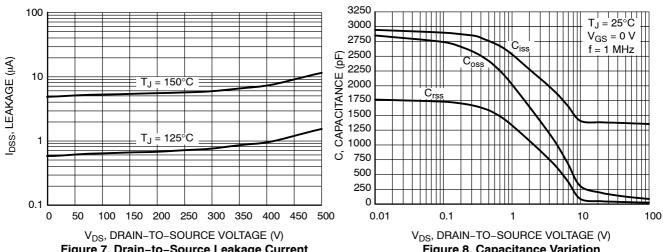


Figure 7. Drain-to-Source Leakage Current versus Voltage

Figure 8. Capacitance Variation

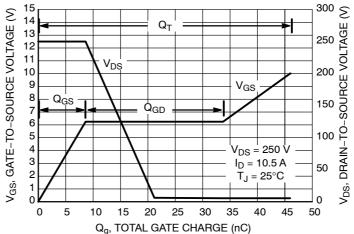


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

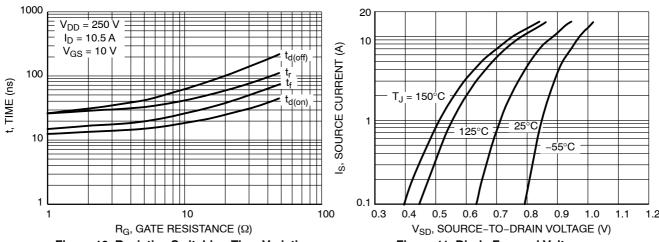


Figure 10. Resistive Switching Time Variation versus Gate Resistance

Figure 11. Diode Forward Voltage versus Current

TYPICAL CHARACTERISTICS

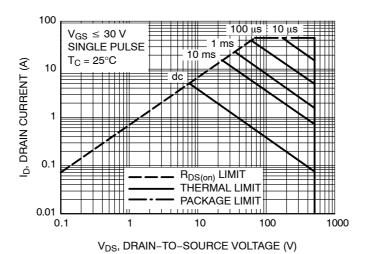


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDF11N50Z

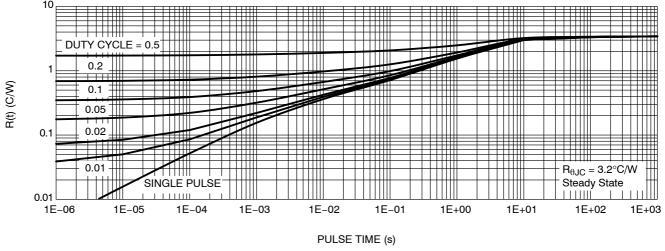


Figure 13. Thermal Impedance (Junction-to-Case) for NDF11N50Z

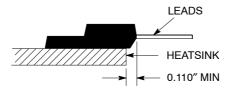


Figure 14. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

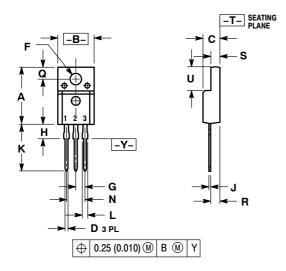
*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

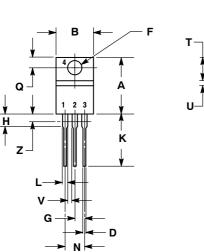
Order Number	Package	Shipping
NDF11N50ZG	TO-220FP (Pb-Free)	50 Units / Rail
NDP11N50ZG	TO-220AB (Pb-Free)	50 Units / Rail (In Development)

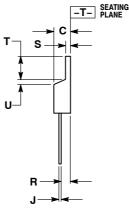
PACKAGE DIMENSIONS

TO-220FP CASE 221D-03 **ISSUE K**



TO-220 CASE 221A-09 **ISSUE AF**





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH
- 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.617	0.635	15.67	16.12	
В	0.392	0.419	9.96	10.63	
С	0.177	0.193	4.50	4.90	
D	0.024	0.039	0.60	1.00	
F	0.116	0.129	2.95	3.28	
G	0.100 BSC		2.54 BSC		
Н	0.118	0.135	3.00	3.43	
J	0.018	0.025	0.45	0.63	
K	0.503	0.541	12.78	13.73	
L	0.048	0.058	1.23	1.47	
N	0.200	0.200 BSC		BSC	
Q	0.122	0.138	3.10	3.50	
R	0.099	0.117	2.51	2.96	
S	0.092	0.113	2.34	2.87	
U	0.239	0.271	6.06	6.88	

PIN 1. GATE

2. DRAIN

SOURCE

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
- CONTROLLING DIMENSION: INCH.
 DIMENSION Z DEFINES A ZONE WHERE ALL **BODY AND LEAD IRREGULARITIES ARE** ALLOWED

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.405	9.66	10.28	
С	0.160	0.190	4.07	4.82	
D	0.025	0.035	0.64	0.88	
F	0.142	0.161	3.61	4.09	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.155	2.80	3.93	
J	0.014	0.025	0.36	0.64	
K	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.39	
Т	0.235	0.255	5.97	6.47	
U	0.000	0.050	0.00	1.27	
٧	0.045		1.15		
Z		0.080		2.04	

STYLE 5: PIN 1.

GATE

2. DRAIN 3. SOURCE

DRAIN

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